20Gbps/ch Optical Interconnection between SERDES Devices over Distances from Chip-to-Chip to Rack-to-Rack

J.Sakai (1), A.Noda (1), M.Yamagishi (2), T.Ohtsuka (3), K.Sunaga (3), H.Sugita (3), H.Takahashi (1), M.Oda (1), H.Ono (1), K.Yashiki (1), H.Kouta (1)

1 : Nano Electronics Research Laboratories, NEC Corporation,

1753, Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa, 211-8666, Japan, j-sakai@bk.jp.nec.com,

2 : Device Solutions Division, NEC Engineering Ltd.

3 : Device Platforms Research Laboratories, NEC Corporation

Abstract

20-Gbps signal transmission of up to 100m between two SERDES devices has been demonstrated using newly developed driver and receiver ICs tuned to the characteristics of VCSELs, photodiodes, and electrical transmission line with which they are used.

Introduction

LSIs for high-end computing systems after 2010 are forecasted to have 20Gbps 1000 signal inputs/outputs (I/Os) [1]. To achieve such higher data throughput and interconnect densities at intra/inter board and rack, optical interconnection technology has been developed.

Optical interconnections above 10 Gbps have been demonstrated between optical ICs, such as driver and receiver ICs [2]. In actual computing systems over 20Gbps/ch, not only the signal properties of optical interconnections but also those of electrical transmission lines between serializer/deserializer (SERDES) devices and optical ICs have to be taken account, because signal degradation and jitter accumulation in the electrical transmission path influence total signal integrity.

Previously, we designed an LSI unit for 1000 channel I/Os (Fig. 1) [3]. The optoelectronic modules were downsized and densely packed in order to be placed near the LSI, this helps to reduce transmission loss. And we developed high speed vertical-cavity surface-emitting laser (VCSEL) and PIN-photodiode (PD) array that fit the high density LSI unit configuration [4].

We have since developed driver and receiver ICs suitable for over-20Gbps optical interconnections and for the LSI unit configuration described above. Each IC is optimally tuned to the characteristics of the PD and VCSEL. 2R functions (reamplification, reshaping) of ICs, along with an equalizer of LSI, are designed to compensate for signal degradation in electrical lines. Further, we have fabricated LSI units, and have demonstrated 20Gbps 100m error-free transmission.

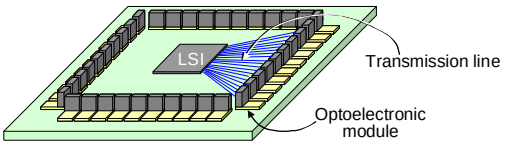

Figure 1: Conceptual model of assembled LSI unit with optoelectronic modules for 1000 channels.

Components and structure

The LSIs are based on 65nm CMOS technology, and each has two I/Os sets for 20 Gbps SERDES. Each transmission (TX) and reception circuit (RX) has a 5-taps feed forward equalizer (FFE) and rear equalizer, respectively. A pseudo random bit sequence (PRBS) generator and a checker for on-chip bit-error-rate (BER) tests are also provided.

We have developed InGaAs quantum well (QW) VCSELs for their high speed and reliability [4]. Their bandwidth was 20 GHz. The PIN-PDs were InP-base back-illuminated mesa-type structure [4]. The 3-dB bandwidth was more than 20 GHz.

Driver and receiver ICs are fabricated in a SiGe-BiCMOS process to meet the requirements of high speed (above 20Gbps) and low power consumption. In our circuit design, electrical equivalent circuit models of VCSEL and PD were introduced to optimize the combined characteristics of ICs and optical devices. IC designs for maximum eye openings at 20Gbps were then determined. Each driver and receiver IC was equipped with an equalizer. The resulting power consumption values for the driver and receiver ICs in our design are, respectively, 250mW and 200mW, half of what they would have been with a GaAs process.

Each TX and RX optoelectronic module was assembled on a 5.0 x 5.0 x 0.45mm alumina substrate with the ICs and the optical devices.

The motherboard is a build-up substrate, which is suitable for high-density wiring. The distance between each LSI and the optoelectronic module is 40mm [3]. In order to reduce line loss, we employed a diagonal pair structure, which made it possible to widen the lines while still maintaining the same characteristic impedance [5]. The S21 at 10GHz was 3.7dB, which is 0.7dB less than that in a conventional stacked pair.

The LSI unit was fabricated by mounting LSIs and TX and RX optoelectronic modules on a motherboard.

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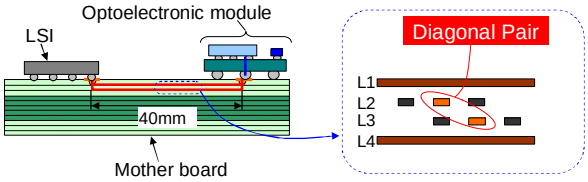


Figure 2: Cross-sectional view of LSI unit

Performance

We measured the frequency domain transmission properties between the LSI and a optoelectronic module ("a" in Fig. 3). This property includes loss in the probe and cable used for the measurement, as well as transmission loss inside the LSI. With respect to this property, the FFE was optimized to maximize the eye opening at 20 Gbps ("b" in Fig. 3). Although total characteristics were relatively flat below 8 GHz, loss drastically increased over 12 GHz, which might be expected to lead to ISI ("c" in Fig. 3).

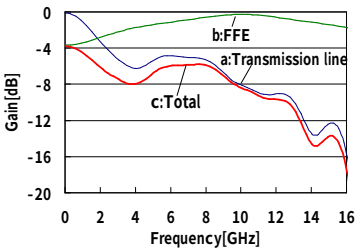
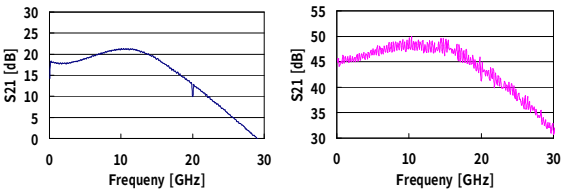


Figure 3: Transmission properties between LSI and optoelectronic module.

Fig. 4 shows the small-signal frequency response of the driver and receiver ICs. The equalizer of each IC is designed to have a peak gain of roughly 11.5 GHz. The 3dB bandwidths of the driver and receiver ICs are, respectively, 18 GHz and 21 GHz.



(a) Driver (b) Receiver

Figure 4: Measured S-parameters of ICs.

LSI-to-LSI signal transmission was carried out with two LSI units placed opposite each other. The VCSEL of one LSI unit was connected to the PIN-PD of the other with GI50 100m multi-mode fiber. 20-Gbps 2^7-1 PRBS data, which corresponds to the 8B/10B that is generally used in actual systems, was transmitted from the LSI.

Fig. 5 shows eye diagrams. The signal shown in Fig.5 (a) is equalized by the LSI and propagated through the substrate. It has a clear eye opening, but the 20-80% rise time is 22.2 ps, which suggest that degradation in the higher harmonics is nonnegligible. The driver IC amplifies this waveform by the above-mentioned frequency response and shapes it by a limiting function, and the VCSEL transmits it through 100m MMF (Fig. 5 (b)). Again the waveform is shaped by the receiver IC. As may be seen in the waveform in Fig. 5 (c), the rise time of the input signal is only 19.5 ps, which means that the 2R functions of driver and receiver ICs have effectively shaped the waveform. An eye opening of 114mV x 29ps is obtained.

Fig. 6 shows BERs measured by the BIST cuircuit equiped on the RX LSI. Error-free (BER < 10^{-12}) transmission was achieved at -6.5dBm average optical power.

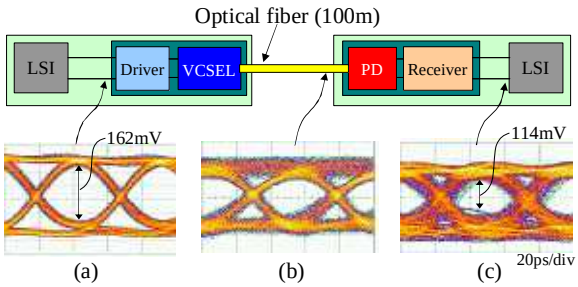


Figure 5: 20Gbps eye diagrams for input signals to driver IC (a), PD (b), and receiver LSI (c).

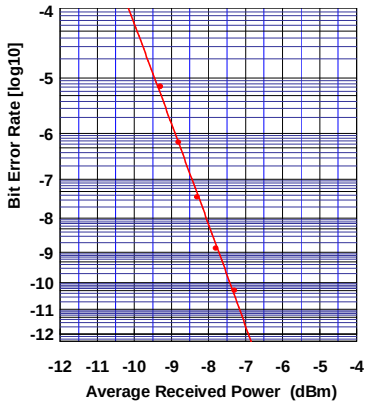


Figure 6: Bit error rate for LSI to LSI transmission.

Conclusions

We have developed optoelectronic modules with driver and receiver ICs tuned for VCSELs, photodiode and electrical transmission property. 20-Gbps signal transmission was successfully demonstrated between two SERDES devices up to 100m. These are applicable to actual high-end computing systems.

Acknowledgements

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