A 1.25/10.3-Gbit/s AC-coupled Dual-rate Burst-mode Receiver without Reset Signals

Kazutaka Hara[1], Shunji Kimura[1], Hirotaka Nakamura[1], Naoto Yoshimoto[1], Makoto Tsubokawa[1], Kazuyoshi Nishimura[2], Makoto Nakamura[3], and Susumu Nishihara[3]
1: NTT Access Network Service Systems Laboratories, NTT Corporation
1-6 Nakase Mihama-ku Chiba-shi, Chiba 261-0023 Japan, E-mail: hara.kazutaka@ansl.ntt.co.jp
2: NTT Microsystem Integration Laboratories, NTT Corporation
3: NTT Photonics Laboratories, NTT Corporation

Abstract We propose and demonstrate a 1.25/10.3-Gbit/s dual-rate burst-mode receiver with two gate circuits to separate the signals according to the bit rate of the input signals. This receiver is cost effective because it employs devices with an ac-coupled interface and no reset signals.

Introduction

Gigabit Ethernet passive optical network (GE-PON) systems are being installed in Japan. 10-Gbit/s-class PON systems and burst-mode transceivers are now being actively investigated for future broadband access networks [1]. To migrate from GE-PON systems to 10-Gbit/s-class PON systems smoothly, the coexistence of GE-PON and 10G-EPON systems as shown in Fig. 1 is indispensable and the specifications of such systems are being standardized by IEEE802.3av TF [2]. The most difficult technical issue as regards coexisting PON systems is to realize a dual-rate burst-mode receiver that can handle both 1.25- and 10.3-Gbit/s upstream signals. The conventional serial-type multi-rate receiver handles only integral multiples signals (e.g. 2.5 and 10 Gbit/s) by using an over-sampling technique in a clock and data recovery circuit (CDR) [3]. Because 1.25- and 10.3-Gbit/s signals must be handled in coexisting systems, the conventional multi-rate receiver suffers from the frequency instability of the CDR. Therefore, a dual-rate receiver is required to employ a parallel-type configuration by which the received signals are sent to each CDR according to its bit rate.

This paper proposes a 1.25/10.3-Gbit/s parallel-type dual-rate burst-mode receiver with two gate circuits (GC) that separates the signals according to the bit rate of the input signals to eliminate the frequency instability of the CDR. This receiver can realize the cost-effectiveness required for access networks by using a trans-impedance amplifier (TIA) and a limiting amplifier (LA) with an ac-coupled architecture and without reset signals. We demonstrate the feasibility of the dual-rate burst-mode receiver and evaluate its sensitivity, dynamic range, and instantaneous response for 1.25- and 10.3-Gbit/s signals.

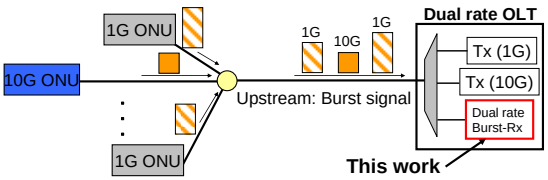

Figure 1: Coexisting GE-PON and 10G-EPON system.

Configuration of Receiver and Circuit Design

Figure 2 (a) shows the configuration of the dual-rate burst-mode receiver. The components of this receiver are an avalanche photodiode (APD), a TIA, a 1G-LA, a 10G-LA, a bit rate discrimination circuit (BDC) for automatically discriminating the bit rate of input signals, and two GCs. Each GC outputs an input signal only when the gate signal from the BDC is input into the GC. So, each 1G- and 10G- signal can be correctly input into each 1G- and 10G-CDR, respectively. Figure 2 (b) shows a schematic diagram of the 1G- and 10G-LA. Both consist of 2-stage LAs and two average detectors (ADs). The ac-coupled architecture for the input interface can be realized by using AD1, which is based on the baseline-wander common-mode rejection (BLW-CMR) technique [4, 5]. LA2 with AD2 improves the duty-cycle distortion caused by the wandering reference voltage, namely the inverted distortion technique, and can achieve an instantaneous response with a high tolerance to consecutive identical digits [5]. Figure 2 (c) shows a schematic diagram of our TIA. Because our TIA uses a dummy core to fix the reference voltage of its output buffer and the LA employs ADs, the reset signals required for a conventional burst-mode receiver can be eliminated.

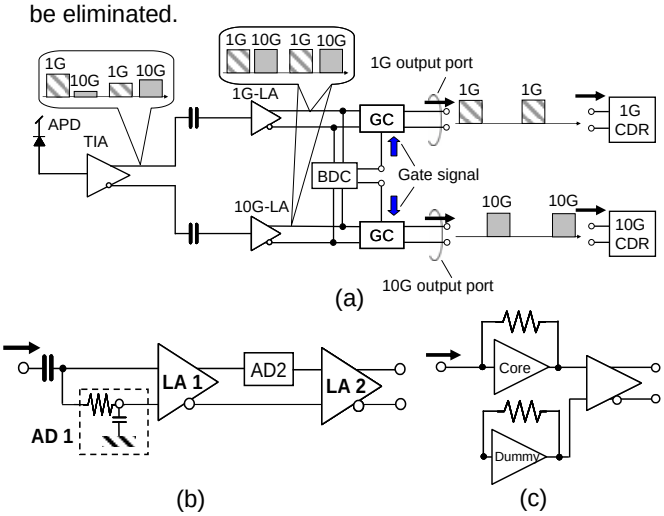

Figure 2: (a) Configuration of our dual-rate receiver, (b) schematic diagram of LA, and (c) TIA.

978-1-4244-2229-6/08/$25.00 ©2008 IEEE

Experimental set-up and results

We evaluated our dual-rate burst-mode receiver with the experimental set-up shown in Fig. 3. Optical burst signals output from optical transmitters (Tx #1 and Tx #2) had bit rates of 10.3 and 1.25 Gbit/s, respectively, with a 2^7-1 PRBS, a preamble length of 75 ns, a payload length of 1280 ns, and a guard time of 100 ns. In this experiment, to confirm the feasibility of the GC, external gate signals output from pulse pattern generator (PPG) #3 instead of the BDC were input into the GCs. When the external gate signal for the 10G signal had a high voltage, the 10G GC output the 10-G signal. We used a 10G-LA and a low pass filter (900 MHz) instead of a 1G-LA.

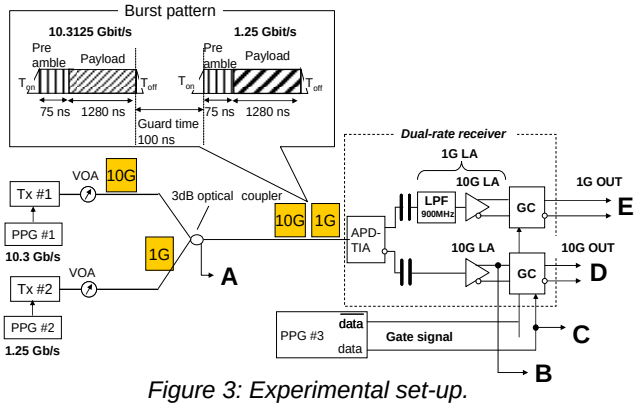

Figure 3: Experimental set-up.

Figure 4 (a) shows waveforms at the measurement points shown in Fig. 3. “A” shows the waveform of the optical 1.25- and 10.3-Gbit/s signals coupled by the 3-dB optical coupler. “B” shows the output waveform from the 10G-LA. “C” shows the external gate signal. “D” shows the output waveform from the “10G output port”. “E” shows the output waveform from the “1G output port”. We confirmed that 10G and 1G signals were output from the “10G output port” and “1G output port”, respectively. Figure 4 (b) shows the bit error rate (BER) characteristics of the burst-mode signals at 10.3 and 1.25 Gbit/s output from the GC. The APD multiplication factor was set to the optimum value according to the input power to avoid the saturation of the APD. For the 1.25-Gbit/s signal, we obtained a receiver sensitivity of -30 dBm, an input overload of more than -3 dBm at a BER of 10^{-12}, and a dynamic range of 27 dB. For the 10.3-Gbit/s signal, we realized a sensitivity of -24 dBm, an input overload of -7 dBm at a BER of 10^{-3}, which corresponds to a BER of 10^{-12} by using forward error correction (FEC), and a dynamic range of 17 dB. The response time of the APD-TIA and 10G-LA was 25 ns and that of the GC was 1 ns in the experiment using 10.3-Gbit/s burst-mode signals. Therefore, the total response time of this receiver was only 26 ns.

Discussion

The dashed line in Fig. 4 (b) shows the calculated BER characteristic of the 10.3-Gbit/s signal estimated from the experimental result obtained for the 1.25-Gbit/s signal. The power penalty at a BER of 10^{-12} between the dashed line (calculated result) and the solid line (experimental result) is about 7 dB. This penalty is caused by the bandwidth degradation of the TIA and the LA, and not by an increase in the speed of the ADs, because good BER performance was obtained for a 1.25 Gbit/s signal with a 2^7-1 PRBS. Therefore, improving the bandwidths can eliminate this penalty and achieve the minimum sensitivity of -26 dBm at a BER of 10^{-3}, which is the IEEE 802.3av specification.

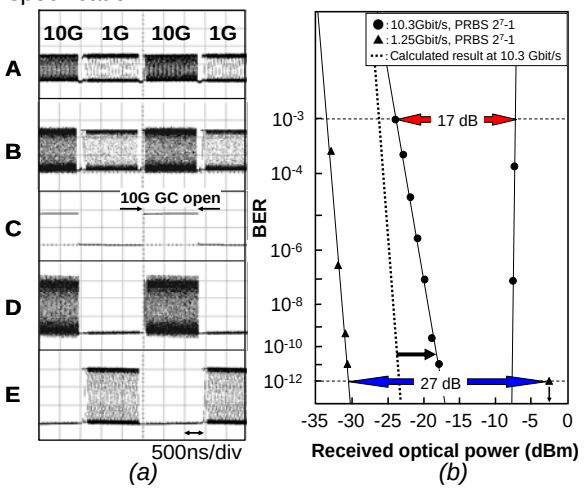

Figure 4: (a) Waveforms at measurement points as shown in Fig. 3, and (b) BER characteristics.

Conclusions

We proposed a 1.25/10.3-Gbit/s parallel-type dual-rate burst-mode receiver with two GCs for separating signals according to their input bit rate. This receiver realized the cost-effectiveness required for access networks by using a TIA with a fixed reference voltage and an LA with two ADs based on BLW-CMR techniques, which employ an ac-coupled architecture and do not need reset signals. We demonstrated the feasibility of our receiver and evaluated its sensitivity, dynamic range, and instantaneous response for 1.25- and 10.3-Gbit/s signals. For the 1.25-Gbit/s signal, we achieved a receiver sensitivity of -30 dBm, and a dynamic range of 27 dB at a BER of 10^{-12}. For the 10.3-Gbit/s signal, we realized a receiver sensitivity of -24 dBm, and a dynamic range of 17 dB at a BER of 10^{-3}. The response time of this receiver was only 26 ns. Our dual-rate burst-mode receiver will contribute greatly to future coexisting GE-PON and 10G-EPON systems.

References

1. S. Nishihara et al., J. Lightwave Technol., vol.26, pp. 99-107, 2008.
2. IEEE P802.3av TF, http://www.ieee802.org/3/av/
3. Pyung-Su Han et al., IEEE Transactions on circuits and systems, Vol. 54, NO. 1, 2007
4. H. Nakamura et al., OFC2008, PDP26, 2008.
5. S. Kimura, submitted to OECC /ACOFT 2008.