All-Optical Static RAM Cell with Read/Write functionality at 5 Gb/s

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Abstract *We demonstrate an optical static RAM cell that comprises two SOA-based switches and an integrated SOA-MZI Flip-Flop, providing random access read/write functionality at 5 Gb/s.*

Introduction

Despite the proven high-speed potential of optical signal processing circuitry, photonic processing devices still experience several difficulties in convincing about their functional potential, one main reason for this being the absence of a reliable optical Random Access Memory (RAM). Optical memory has to overcome innate limitations enforced by the neutral charge of light particles that impedes their storage, making it impossible to mimic the respective electronic memory modules that rely on the negative electron charge. To this end, optical buffering has so far mainly relied on fiber-delay lines or fiber-loop based schemes with limited functional potential. Optical bit-level storage without random access capabilities has been recently demonstrated by means of integrated optical memory elements relying on coupled semiconductor lasers [1],[1], or coupled interferometric switches [3]. However, photonic RAM functionality has been presented only by means of parallelized electronic RAM configurations [4], whereas a truly all-optical RAM design that will provide on-demand storage and retrieval of high-speed optical data has not been addressed so far.

In this article, we demonstrate for the first time to our knowledge an all-optical static RAM cell that provides true random access Read/Write functionality at 5 Gb/s. The proposed optical RAM cell consists of two Semiconductor Optical Amplifiers (SOA) and a hybridly integrated optical flip-flop relying on two coupled SOA-Mach-Zehnder Interferometric (MZI) switches [3]. The SOAs operate as Cross-Gain Modulation (XGM) switches controlling access to the flip-flop configuration, whereas the optical flip-flop serves as the 1-bit memory element. Error-free Read and Write functionality with true random access properties at 5 Gb/s are demonstrated directly in the optical domain.

Experimental Setup

Fig. 1(a) depicts the experimental configuration of the optical static RAM cell. It consists of two SOAs and a hybridly integrated optical flip-flop [3] that uses two CW input signals at λ0 (1559nm) and λ1(1556nm). The logical value of the memory cell is determined by the wavelength of the dominant CW signal [3]. Flip-flop output signals emerge at FF#1 and FF#2 ports and exit the RAM cell through o/p1 and o/p2 after

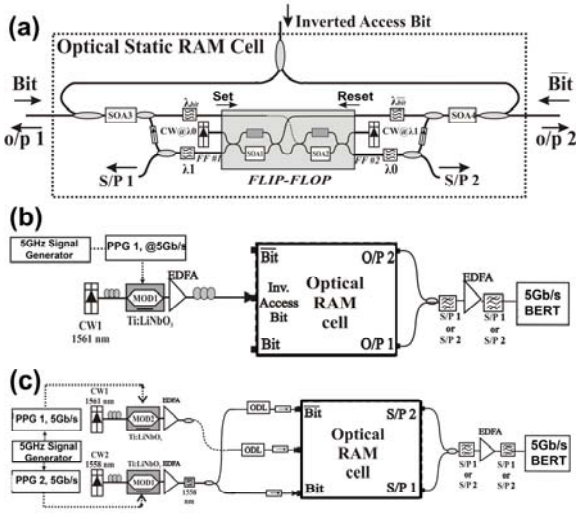

Figure 1: (a) The experimental layout of the optical static RAM cell, (b) the Read mode experimental setup, and (c) the Write mode experimental setup.

passing through SOA3 and SOA4, respectively, when the RAM cell operates in Read mode. When Write mode operation is targeted, the Bit and $\overline{Bit}$ streams enter the RAM cell via SOA3 and SOA4, respectively, and are inserted into the flip-flop acting as the Set and Reset signals [3]. In this way, the flip-flop alters its dominant wavelength state storing the new incoming binary value, whilst the memory content at λ0 and its inverted signal at λ1 are recorded at the State ports S/P2 and S/P1, respectively. Random access operation of the RAM cell in both Read and Write mode operation is provided by the inverted Access Bit that inputs the RAM element through SOA3 and SOA4. As such, SOA3 and SOA4 serve as XGM-based ON-OFF switching devices driven by the inverted Access Bit. A "1" inverted Access Bit value saturates both SOA3 and SOA4 and prohibits the memory content to emerge at the memory outputs o/p1 and o/p2 when operating in Read mode, whereas in Write mode operation it restrains the incoming, co-propagating Bit and $\overline{Bit}$ signals from entering the memory cell and modifying its content. To this end, communication between the memory cell and the outer world can not be established unless the inverted Access Bit becomes a logical "0".

Fig. 1(b) shows the experimental setup used for the performance analysis of the RAM cell in Read mode operation. A CW signal at 1561nm was launched into

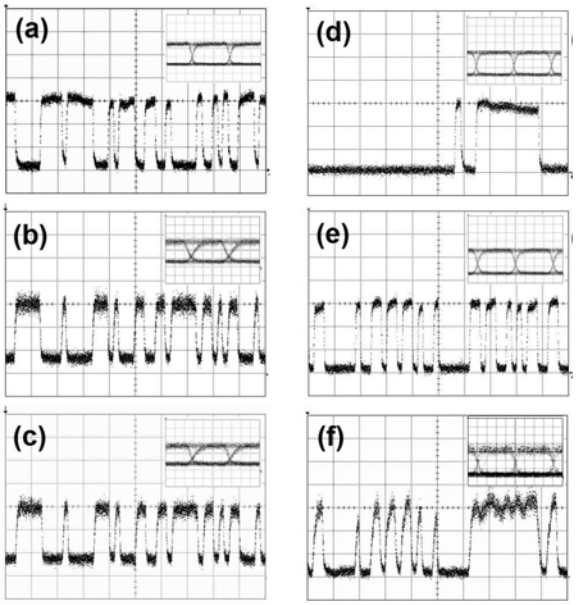

Figure 2: (a), (b), (c) Read mode operation: (a) inverted Access bit, (b) Read output at o/p2, (c) Read output at o/p1. (d), (e), (f)) Write mode operation: (d) inverted Access bit, (e) incoming *Bit*, (f) RAM cell memory content recorded at S/P1 (λ1). Time scale: 1ns/div for traces, 50ps/div for the eye diagrams shown in the insets.

a Ti:LiNbO3 modulator (MOD1) driven by a PRBS pattern generator, yielding a 5 Gb/s 2^9-1 NRZ data sequence at its output that was used as the inverted Access Bit signal into the RAM cell. Fig. 1(c) depicts the experimental setup used when Write operation is intended. The inverted Access Bit signal was generated in a way similar to Fig. 1(b). For the Bit and $\overline{Bit}$ signal generation, a CW signal at 1558nm entered MOD2 that was driven again by a 2^9-1 PRBS generator, so as to obtain a 5 Gb/s NRZ data signal with successive 500-bit long data parts of inverted logical values. This signal was then split into two fiber branches and was injected as the Bit and $\overline{Bit}$ sequences into the RAM cell after a 500-bit differential delay between the two branches.

Results and Discussion

Fig.2 shows the experimental results for the optical static RAM cell at 5 Gb/s. The left column illustrates the results obtained when operating in Read mode, whereas the right column depicts the Write mode results. Fig. 2(a) shows the pulse trace and the eye diagram of the inverted Access Bit entering the RAM cell, whereas Fig. 2(b) and (c) present the respective Read output signals obtained at o/p2 and o/p1 for the two different flip-flop states with λ0 and λ1 dominant wavelengths, respectively. In both flip-flop states, successful Read operation is confirmed by the complementary values of the corresponding Read output signals and the inverted Access Bit stream. Write mode operation is verified by the pulse traces and eye diagrams shown in Fig. 2(d), (e) and (f) that depict the inverted Access Bit, the incoming Bit and the λ1 memory content that emerges at S/P1 port, respectively. As long as the inverted Access Bit is "0",

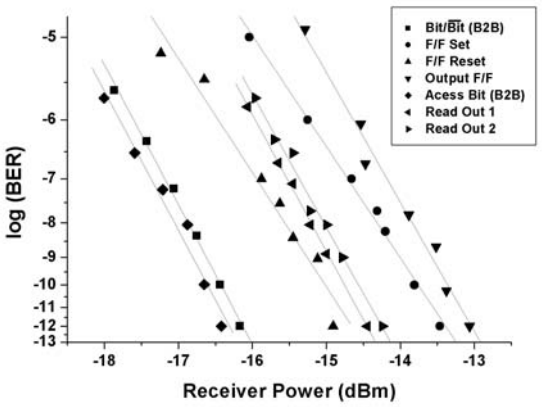

Figure 3: BER measurements at 5 Gb/s for Read and Write mode operation.

the incoming Bit stream passes unaffected through SOA3 serving as the Set signal for the flip-flop, whilst the $\overline{Bit}$ data stream travels through SOA4 and acts as the respective Reset signal. This leads to the successful storage of the incoming Bit signal as it is being imprinted on λ1 and exits through S/P1, as shown by Fig. 2(f). The memory content retains its last value and is not modified whenever the inverted Access Bit is a logical "1", since both Bit and $\overline{Bit}$ signals are blocked resulting to a logical "0" both for the Set and Reset signal values. Fig. 3 shows the BER curves obtained for the incoming 5 Gb/s inverted Access Bit, Bit / $\overline{Bit}$ and the corresponding Set and Reset signals, as well as for the two Read mode output signals and the λ1 memory content in Write mode conditions. Error-free operation was obtained for both Read and Write mode RAM operation with a power penalty of less than 2 and 3 dB, respectively. Operating conditions for the optical flip-flop were 1dBm and 5.5dBm average optical power for the two CW signals and 6.5dBm and 8.8dBm peak power values for the Set and Reset signals, respectively.

Conclusion

We have presented true Random Access Read and Write memory functionality at 5 Gb/s utilizing two SOA-based switches and a hybridly integrated optical flip-flop. Given that the 5 Gb/s speed limit is mainly determined by the time-of-flight between the coupled SOA-MZI switches, the remarkable progress of Silicon Photonics could possibly enable integrated optical RAM with access rates beyond 40 Gb/s.

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