# High Capacity Demonstration of a Compact Regrowth-Free Integrated $4 \times 4$ Quantum Well Semiconductor Optical Amplifier Based Switch 

H. Wang, E.T. Aw, M.G. Thompson, A. Wonfor, R.V. Penty, I.H. White<br>Electrical Division, Department of Engineering, University of Cambridge, 9 JJ Thomson Ave, Cambridge, CB3 OFA, UK hw288@cam.ac.uk


#### Abstract

A fibre-to-fibre lossless integrated $4 \times 4$ SOA switch achieves an IPDR $\sim 6 \mathrm{~dB}$ at $<2 \mathrm{~dB}$ penalty for $8 \lambda \times 10 \mathrm{~Gb} / \mathrm{s}$. $10 \mathrm{~Gb} / \mathrm{s}$ cascaded operation of two $4 \times 4$ switches is demonstrated.


## Introduction

The demand for higher bandwidths in high performance systems such as server backplanes has encouraged research into the use of photonics as the switching technology. Semiconductor optical amplifiers (SOAs) have attracted much interest owing to their ability for lossless switching of high capacity data with nanosecond timescales. Larger switches can be built by cascading $2 \times 2$ or $4 \times 4$ switching elements. To date several integrated $4 \times 4$ SOA switches have been demonstrated [1-2]. The use of SOA switches in WDM interconnect system for optical interconnect system such as server backplanes have been demonstrated with the use of discrete SOA switches [3]. In this paper, we investigate the feasibility of a compact, monolithically integrated non-blocking $4 \times 4$ AIGalnAs QW SOA based switch for high capacity, high port count network applications. Despite using integrated reflectors to allow a compact form, and not requiring re-growth fabrication, lossless fibre-to-fibre performance is achieved.

## Device Details



Figure 1: Schematic of $4 \times 4$ switch topology.
The switch active region incorporates a 5 AIGalnAs QW active structure which is grown on an $\operatorname{InP}$ substrate using MBE. Standard photolithography and ICP dry etch processes are used to fabricate ridge waveguide structures. Each of the four input and output ridge waveguides has a width of $2 \mu \mathrm{~m}$. Integrated beamsplitters and mirrors are formed using deep etching to form vertical sidewalls through the active region. The lengths of the paths through the switch range from 1.55 mm (for e.g. path

1 to 1 ) to 2.8 mm (for e.g. path 1 to 4 ), as shown in Figure 2. The chip has a very compact footprint of $2.04 \mathrm{~mm} \times 1.54 \mathrm{~mm}$.


Figure 2: Schematic of the $4 \times 4$ switch showing the beamsplitters, mirrors, and longest/shortest paths.

## High Capacity Operation

Figure 3 shows the spectral gain of the $4 \times 4$ switch when biased at high currents of $300 \mathrm{~mA}, 70 \mathrm{~mA}$ and 350 mA at the input, gating and output SOA sections respectively for the longest and shortest paths through the switch. A 3dB gain bandwidth of around 30 nm is observed. A switching rise time of 6 ns and a fall time of $3 n s$ have been achieved, limited by parasitic effects.


Figure 3: Gain spectral for longest \& shortest paths
The input power dynamic range (IPDR) of the switch is investigated for an $8 \lambda \times 10 \mathrm{~Gb} / \mathrm{s}$ DWDM input to assess the switch performance for high capacity data routing. The test bed is shown in Figure 4. The transmitter comprises eight DWDM lasers, with
wavelengths from 1547 nm to 1555 nm with 0.8 nm spacing, modulated at $10 \mathrm{~Gb} / \mathrm{s}$ with a $2^{31}-1$ PRBS sequence. Each channel is decorrelated using either an electronic or fibre delay. Owing to the polarisation dependence of the device, polarisation controllers are used to set the input signal to TE polarisation prior to the switch. At the receiver module, the channel at 1550.9 nm is selected using an AWG and the bit error rate (BER) curves are measured using a BER tester.


Figure 4: $8 \lambda \times 10 \mathrm{~Gb} / \mathrm{s}$ DWDM Test bed
The IPDR at a BER of $10^{-9}$ is shown in Figure 5. It can be observed that all of the paths measured have an input power dynamic range (IPDR) of $>6 \mathrm{~dB}$ for a power penalty below 2dB. Measurements at high input power are limited by the available laser output power. Paths with longer output SOA length suffers from narrowed IPDR because the high gain saturates the switch at lower input powers when compared to paths with shorter SOA length.


Figure 5: $8 \lambda \times 10 G b / s$ IPDR results of the switch

## Potential for High Port Count Applications

Large port count switches can be formed by cascading one or more $4 \times 4$ switches. For example, a blocking $16 \times 16$ switch can be built from eight $4 \times 4$ arranged in two switch cascades whilst a nonblocking $16 \times 16$ can be built from twelve $4 \times 4$ arranged in three switch cascades. Figure 6 shows the unsaturated fibre to fibre gain of the $4 \times 4$ switch at wavelength 1550.9 nm for different ports as a function of switching current for the gating SOAs. The paths shown represent the shortest path (1-1 and 1-4) and longest path (1-4 and 4-1) through the switch. The input and output SOA sections are each biased at a current of 150 mA and 300 mA respectively. The difference in gating current characteristics can be controlled using electronic control schemes to ensure a uniform output powers [4]. A maximum fibre to fibre gain of 5 dB is observed for the longest path and 0 dB for the
shortest path. As a total of -6.3 dB coupling loss is measured, a very high net gain can be achieved in an integrated cascaded environment. Cascaded performance is investigated by transmission of 1 channel at $10 \mathrm{~Gb} / \mathrm{s}$ through a cascade of two $4 \times 4$ switches. The result is shown in Figure 7. For this cascade, a 6 dB dynamic range at power penalties below 2 dB , with minimum penalty of 0.8 dB is achievable.


Figure 6: Unsaturated gain for various SOA gating currents


Figure 7: IPDR for two $4 \times 4$ cascade at $10 \mathrm{~Gb} / \mathrm{s}$

## Conclusions

A compact, monolithic $4 \times 4$ SOA switch is shown to have potential for high capacity, high speed switching applications. A switching speed of 6 ns rise time and 3 ns fall time is measured. This switch achieves a maximum fibre to fibre gain of 6 dB . BER measurements on the worst and best case path at $8 \lambda \times 10 \mathrm{~Gb} / \mathrm{s}$ shows an IPDR of $>6 \mathrm{~dB}$ (with minimum penalty of 1.2 dB ). Cascaded operation at $10 \mathrm{~Gb} / \mathrm{s}$ also shows IPDR of 6 dB at power penalties $<2 \mathrm{~dB}$, illustrating the potential for these switches to enable a $16 \times 16$ switch. These results shows the potential of the integrated $4 \times 4$ switch for high speed, high capacity optical switching applications.

## References

1. van Berlo et al, IEEE Photonics Tech. Lett., vol.7, no.11, pp.1291-1293, Nov 1995
2. J.-H. Song et al., Japanese J. of Appl. Phys., Vol. 43, no. 1A/B, pp. L18-20, 2004
3. T. Lin et al., J. of Lightwave Tech., vol.25, no. 3 pp.655-663, March 2007
4. E.T. Aw, et al, ECOC 2006, paper Th1.2.5
