Hybrid Flip-Chip Integration of a 40 Gb/s DPSK Receiver Comprising a Balanced Photodetector on a DLI-SOI Board

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Abstract

A DPSK receiver concept using flipchip hybrid integration of InP photodetectors on SOI boards with optical decoder is presented. Horizontal waveguiding enables low-cost production for high data rates.

Introduction

Novel data modulation formats such as Differential Phase Shift Keying (DPSK) currently replace traditional On-Off Keying (OOK) and duobinary modulation. Receivers for PSK data signals include an optical decoder to detect phase differences between consecutive bits of data. Such decoder can be assembled by free space optics, fiber configurations or in planar waveguide technology. At present PSK receivers have to be assembled from separate products. The widespread application of PSK modulation formats requires new cost-efficient receiver configurations. Therefore monolithic integration, i.e. on InP is an objective currently investigated [1]. In this paper a hybrid integration on a planar lightwave circuit (PLC) board is proposed, comprising optical decoding and flip-chip components for detection and pre-amplification. The receiver set-up is designed for 40 Gb/s DPSK at an operation wavelength in the C-Band.

Planar integration concept

Hybrid flip-chip integration offers the possibility to combine the advantages of both material systems InGaAsP for performance and silicon on insulator (SOI) for price and volume production. The proposed DPSK receiver set-up comprises an optical waveguide network building a 1 bit delay interferometer (DLI) as optical decoder [2], and a balanced photodetector chip (BPD), which is mounted onto the SOI board by flip-chip (FC) technique. The complete design follows a linear signal guiding approach to avoid any signal redirection which eases the assembly technologies. In a second step a SOA will be integrated using the same concept and technology, which results finally in a zero-loss small size DPSK receiver.

The complete PLC will be mounted into a small size- package with a footprint of 58x28 mm. The RF-connection is accomplished by a CPW RF line onto the PLC between the PD chip and the RF connector at the package to enable a broad bandwidth operation. The complete receiver set-up and the profile of a mounted flip-chip BPD on an SOI Board are shown in Fig. 1a, b.

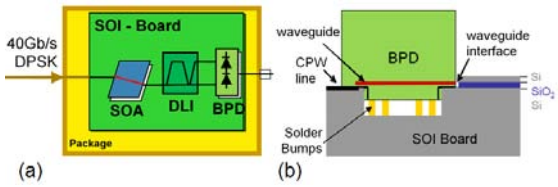

Figure 1a: The 40 Gb/s DPSK receiver concept, 1b: schematic profile of a flip-chip BPD – SOI board assembly.

SOI board with waveguide network

The optical network is based on strong optical coupling rib waveguides with (3.5 x 4 µm). SOI rib waveguides are particularly well suited for the trimming of the polarization dependence. Silicon does not exhibit any material birefringence, while the choice of rib geometry and cladding overlay leave two independent parameters for birefringence tuning. This technique is used to build optical networks with a low polarization dependency. Recently, state-of-the-art performance was demonstrated for the DPSK demodulator on SOI with a record-low polarization dependence of 0.4 GHz [2].

The optical waveguides lead the signals to the edge of an integration zone, where the flip-chip BPD is placed. The SOI waveguides have lateral optical tapers to expand to optical field for an efficient coupling at the interface to the BPD. The integration zones contain solder bumps, alignment standoffs, and electrical fan-out structures with RF-capability.

Flip-Chip Integration

Photodetectors with topside down layout regarding mechanical, electrical and optical issues are required for hybrid integration. The FC BPD bases on the design of high-speed waveguide integrated photodetectors, for which bandwidths of up to

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70 GHz have been achieved [3]. The diodes are grown by a one-step MOVPE process on a semi-insulating InP substrate. Balanced pin-diodes (active area 4.5x15 μm^2) employ evanescent coupling from a monomode rib waveguide. To reduce coupling losses the waveguides comprise monolithic integrated tapers, which are finally antireflection coated.

This structure was modified for flip-chip purpose. At first, the BCB pin mesa passivation was adapted, together with an enhanced metallization scheme for face-down interconnecting. Second, a three-dimensional relief structuring of the chip surface is needed, providing appropriate stand-offs and mechanical delimitations for chip adjustment on the SOI board. Fig. 2 shows the top side of a fabricated device. The following properties of the balanced detector are achieved: responsivity 0.48 A/W, polarisation dependent loss < 0.5 dB, bandwidth > 75 GHz.

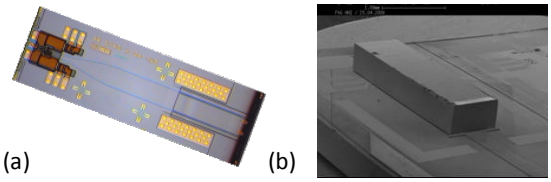

Figure 2a: BPD chip with pads for bump support and 2b: detector chip adjusted to optical and electrical interconnections on the SOI board.

The SOI board is based on a three layer composition. The top silicon layer is used for waveguides and passive optical components, such as the DLI. The buried oxide layer acts as the vertical adjustment plane for the active components. The silicon substrate is etched for the definition of solder bumps and electrical connection. Gold-tin solder bumps are sputtered onto the SOI foundations. The RF connection is implemented by coplanar transmission CPW lines on a high resistive substrate. One end of the RF line is optimized to the FC BPD, whereas the other side is optimized to adapt a standard V-connector to give a complete continuous 50 Ohm design. The optical alignment tolerance of the interconnection between an SOI waveguide and a BPD is 1 µm vertical direction and 2 µm in horizontal direction, (verified by measurements). For the flip-chip procedure, a pick-and-place system with 1 µm accuracy is used. Visual adjustment provides the horizontal alignment, while the vertical position is defined by the delimiters on SOI. The soldering under inert gas takes place at temperatures above 300°C. Fig. 2b shows a FC BPD mounted onto the SOI board.

Investigation of the BPD – SOI Assembly

The very first flip-chip assemblies were investigated in terms of mechanical, optical and electrical parameters. Shear tests show a mechanical strength of up to 5.8 N. A tapered fiber couples the light into the SOI waveguide (Fig. 3a). The coupling is verified by the measurement of the photo current in a two dimensional scan (Fig. 3b).

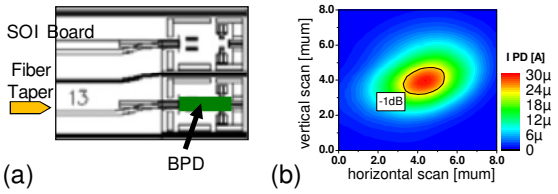

Figure 3a: Flip-chip diode on SOI, 3b: Photo current of a 2D scan for optical coupling with a fiber taper.

The insertion loss measured on these first samples is about 14 dB due to some imperfections in the processing. In the next run it should be reduced down to the design specification of about 5 dB.

In a second step we analysed the RF performance of the BPD-SOI hybrid. The bandwidth of the assembly was determined by an S_{21} measurement to 25 GHz (Fig. 4a), while the value for S_{22} remained below -5 dB (<-10 dB up to the 3dB-bandwidth), cf. to Fig. 4b.

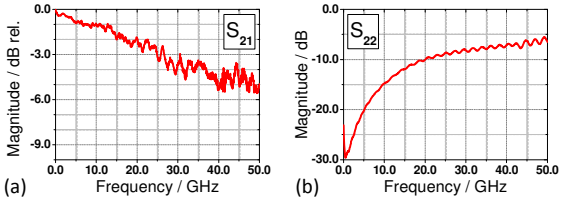

Figure 4a: Measurement of S_{21} and 4b: S_{22}.

Summary and Conclusions

The presented hybrid concept is proposed as an integrated solution for a compact and robust DPSK receiver. The functionality of the integrated DPSK to OOK demodulator and of the flip-chip integrated photodetector is verified, and first, promising results were achieved. Further work will focus on the improvement of the optical coupling and RF bandwidth. A zero insertion loss set-up can be enabled by the integration of a buried heterostructure polarisation independent flip-chip SOA developed in parallel. An RF amplifier chip will be integrated on package level directly after the hybrid.

Acknowledgement

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